Virtex-4 FPGA SEU Mitigation Design Consideration

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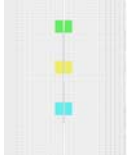
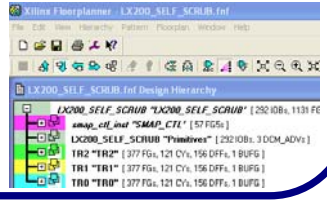
The Virtex-4 QV advantages

Device	SEL	TID	CLB Array	# of Slices	#of LUTs	#of FFs	Distributed RAM bits	Block RAM	# of Blocks	# of Multipliers	# of DCMs/DLLs, PMCDs, PLLs	# of BUFGs	# of Max I/O	# of Max diff pairs	# of Rocket I/Os	# of PPCs	# of EMACs
V4	MeV-cm2/mg	krad															
			4 slices per CLB		4-Input	2 per Slice	2 slices per CLB	18k bits per block		DSP48	DCMs, PMCDs	BUFGs	Max I/O	diff pairs	Rocket I/Os	PPCs	EMACs
LX200	100	250	192 x 116	89,088	178,176	178,176	1,425,408	6,193,152	336	1 96	12, 8	32	960	480	0	0	0
			4 slices per CLB		4-Input	2 per Slice	2 slices per CLB	18k bits per block		DSP48	DCMs, PMCDs	BUFGs	Max I/O	diff pairs	Rocket I/Os	PPCs	EMACs
SX55	100	250	128 x 48	24,576	49,152	49,152	393,216	5,898,240	320	8 512	8, 4	32	640	320	0	0	0
			4 slices per CLB		4-Input	2 per Slice	2 slices per CLB	18k bits per block		DSP48	DCMs, PMCDs	BUFGs	Max I/O	diff pairs	Rocket I/Os	PPCs	EMACs
FX60	100	250	128 x 52	25,280	50,560	50,560	404,480	4,276,224	232	2 128	12, 8	32	576	288	12 or 16	2	4
FX140	100	250	192 x 84	63,168	126,336	126,336	1,010,688	10,174,464	552	2 192	20, 8	32	896	448	24	2	4

Defeat DCE and MBU

- Area Group Overview
  - Slice level control to frame level control
  - Different level of control
  - Timing impact for designs with large number of voters
- Assign Area Group
  - By instance name with wild card
    INST "*_TR0" AREA_GROUP = "AG_TR0";
  - By clocking source: only capture synchronous elements
    - TIMESPEC TS_clkin_TR0=PERIOD "clkin_TR0" TS_clkin_TR0;
    - TIMEGRP "clkin_TR0" AREA_GROUP = "clk_TR0_AG";
- Range Assignment
  - No range assignment simply default to slice level control
  - Could increase routing time. Skip for design with lots of voters
  - AREA_GROUP "AG_TR0" RANGE=SLICE_X0Y0:SLICEX16Y16;
- Close Attribute
  - Could increase routing time
  - Avoid for clocking source based area group
  - Example
    AREA_GROUP "AG_TR0" PLACE=CLOSED;
    AREA_GROUP "AG_TR0" GROUP=CLOSED;





V4 Specific Primitives Usage Consideration

Primitives	Usage Consideration
SRL16 LUTRAM	1. Must enable GLUT_MASK 2. Constant data flush
FIFO	1. Empty and Full flag issues 2. Check Xilinx solution 22462
Half Latch	1. No stuck error 2. Alternative dedicated posts a.Set XIL_MAP_RETAIN_CONSTANT_FF_CTL b.Set XIL_PAR_VCC_HARD1_ONLY
DCM	1. Must disable GLUT_MASK 2. Phase shift for divided output
DCI	1. IO or bank wide failure a.Stuck failure with Continuous and Freeze 2. Robustness: As required, Continuous, Freeze
IDELAY IDELAY_CTL	1. One IDELAY_CTL per bank 2. Single point, bank wide failure
STARTUP	1. Ground CLK, GSR, GTS 2. Tie all USR* ports high

- Regional GLUT_MASK control to be supported in future software
- Dedicated TIEOFF site support
  - ISE: 9.2isp3
  - TMRTool: TBD

Implementation Settings

- XST:
  - Change FSM Encoding Algorithm to "Sequential"
  - Enable Safe Implementation
- MAP:
  - Disable global optimization (default)

General Design Considerations

- TMRTool User Guide
  - Selection IO mitigation
  - DCM divided clock phase matching challenge
  - Asynchronous elements
  - Finite State Machine implementation impact
  - Timing
  - Simulation and hardware verification and many others

Power Saving

- TMR typically equates to 3X power consumption
- Power Reduction option available for XST, Map, and PAR
- Average of 10~15% power reduction
  - Minimize net capacitance
  - Optimize net capacitance routing for non timing critical nets
  - Reprogram LUT to lower internal toggle
- May decrease design footprint as shorter routes are used
- Future Improvements
  - Clock Power reduction
  - Power aware clustering